

Page 4, between lines 2 and 3, insert the heading -- OBJECTS AND SUMMARY OF

THE INVENTION

Page 5, between lines 26 and 27, insert the heading -- BRIEF DESCRIPTION OF THE

DRAWINGS

Page 7, line 17, insert the heading -- DESCRIPTION OF THE PREFERRED

EMBODIMENTS

IN THE CLAIMS

Please amend claims 3, 4, 6, 7, 8, 9, 10 and 11. Following are the claims as amended.

A marked-up version of the changes made to the claims is attached and entitled *Version with Markings to Show Changes Made*.

3. (Amended) Integrated circuit according to claim 1, wherein the means (CC1) for delivering the pulsed modulation signal (S1m4) comprise at least two capacitors (Cref, Cas) and means (WLCC, CG1, CMP, D6, SR1, T1, T2, T3, T4) for:

- charging the first capacitor (Cref) with a constant current (Iref) before the emission of a load modulation pulse, during a time (Tref) fixed by a predetermined number of clock cycles (H),
- charging the second capacitor (Cas) with a constant current (Iref) during the emission of a pulse, and
- stopping the emission of the pulse when the charge voltage (Vas) of the second capacitor is equal to the voltage (Vref) at the terminals of the first capacitor.

4. (Amended) Integrated circuit according to claim 1, comprising means (WLCC) for:

- transforming the binary signal to be transmitted (DTx) into a binary coded signal (S1) presenting at least, at each bit of the binary signal, a rising or falling variation edge, and
- transforming variation edges of the binary coded signal (S1) into load modulation pulses (I1-I<sub>n</sub>) of short duration compared to the duration (T<sub>b</sub>) of a bit of the binary signal to be transmitted (DTx).

6. Integrated circuit according to claim 1, wherein the modulation signal (S1m4) is combined with an a.c. signal (Fsc) in order to form a load modulation signal comprising a.c. signal pulses.

7. Integrated circuit according to claim 1, wherein the load modulation pulses have a duration (T<sub>as</sub>) shorter than or equal to the quarter of the duration of a bit of the binary signal to be transmitted (DTx).

8. Integrated circuit according to claim 1, wherein the clock extraction device (CEC1) is maintained in an inhibited state after the emission a load modulation pulse, at least for a time (T<sub>ref</sub>, T<sub>as</sub>) equal to the duration of a load modulation pulse.

9. Integrated Circuit according to claim 1, wherein the clock extraction device (CEC1) is arranged to extract a clock signal (H) from an a.c. voltage (V<sub>ac</sub>) induced in the antenna coil (L<sub>s</sub>).